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IIC详述

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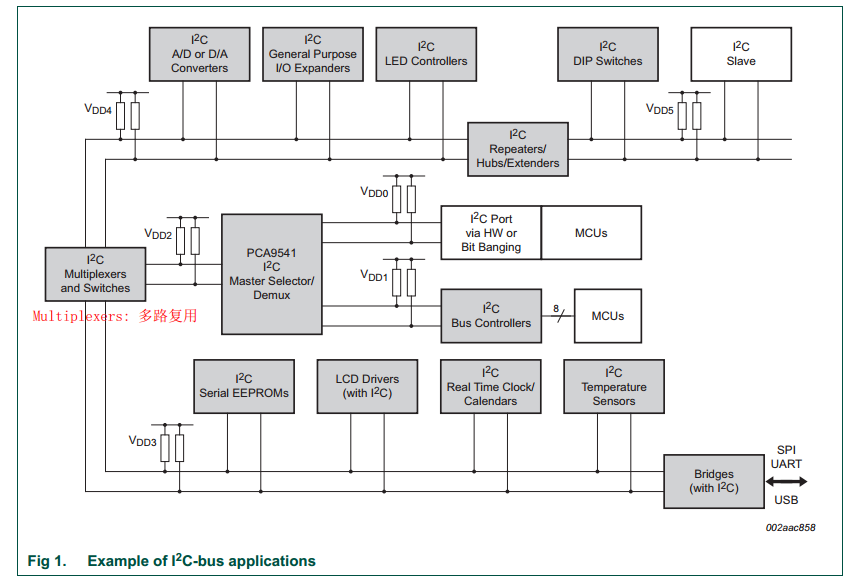
目录

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# IIC概述

IIC Bus 仅需要2个总线：串行数据总线SDA和串行时钟总线SCL。每个接到总线上的设备均是使用软地址来区分。

EXAMPLE：IIC总线应用。



## IIC模式分类

按主从机模式可分为主机和从机。

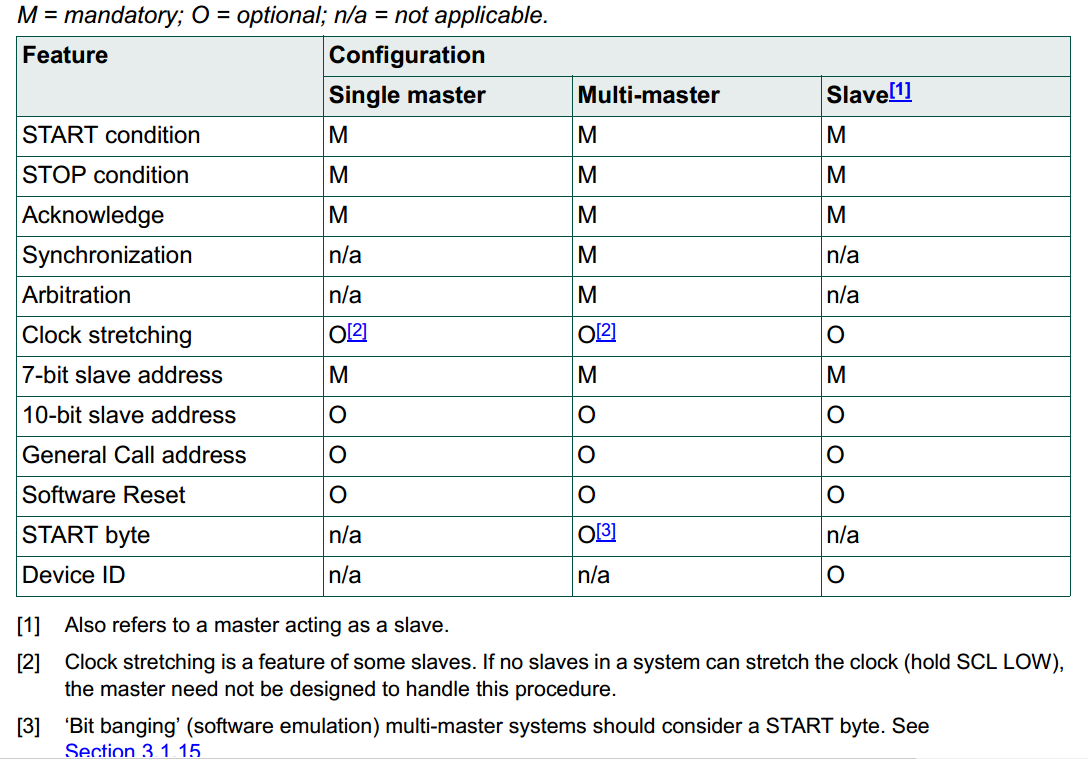
|  |  |
| --- | --- |
| **分类** | **作用** |
| 主设备Master | 产生时钟信号和控制通讯的设备 |
| 从设备Slave | 由主设备控制的设备 |

按传输速率可分为：The Standard-mode、The Fast-mode、The Fast-mode Plus和The High-speed mode。

|  |  |  |
| --- | --- | --- |
| **分类** | **传输速率** | **类型** |
| The Standard-mode | up to 100 kbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Fast-mode | up to 400 kbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Fast-mode Plus | up to 1 Mbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The High-speed mode | up to 3.4 Mbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Ultra Fast-mode | up to 5 Mbit/s | Serial, 8-bit oriented, unidirection data transfers |

## 信号类型

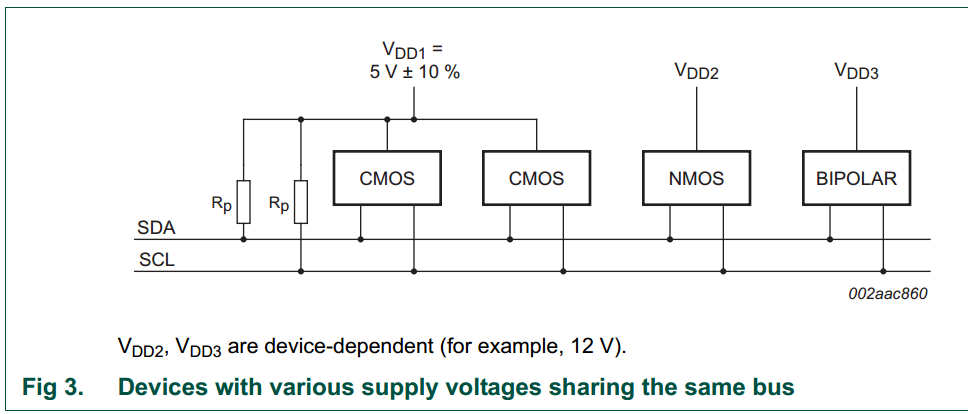
Spplicablity of IIC-bus protocol feastures



### SDA和SCL信号

SDA和SCL总线都是双向通信线。

* 为确保总线为FREE时，SDA和SCL总线为HIGH，SDA和SCL总线**必须通过上拉电阻连接到供电电源上**。
* 为确保实现wired-AND功能，总线设备必须**采用开漏（open-drain）或者集电极开漏（open-collector）方式**。
* 总结设备的接口数量影响总线容值。

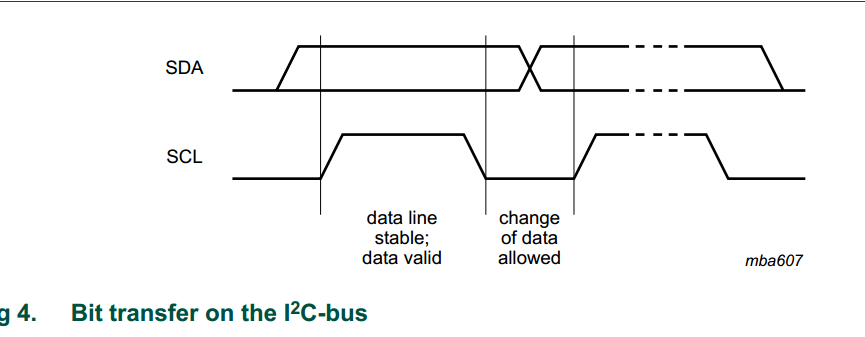


### 逻辑电平

|  |  |
| --- | --- |
| Logic Levels | 电压范围 |
| 0（LOW） | 0.3VDD |
| 1（HIGH） | 0.7VDD |

### 数据有效性

* SCL低电平，允许数据变化
* SCL高电平，允许捕获数据



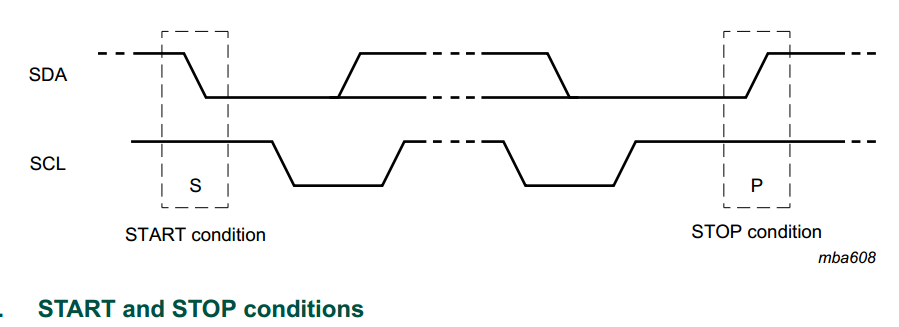
### START和STOP信号

所有的数据通讯起始于START（S），结束于STOP（P）。

* SCL为HIGH时，SDA由HIGH变为LOW，产生START信号。
* SCL为HIGH时，SDA由LOW变为HIGH，产生STOP信号。

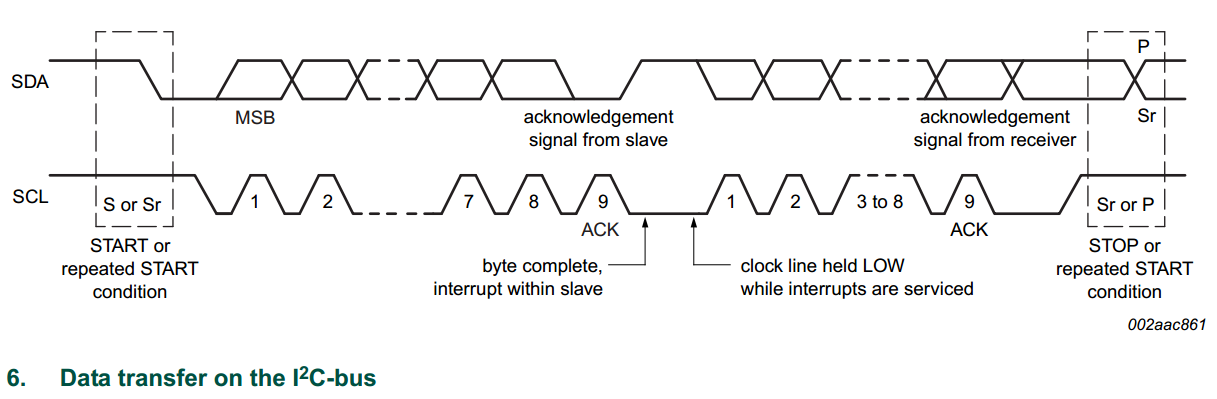
**NOTE**：

START和STOP均由Master主设备产生。



### Byte格式

* SDA的每个字节必须为8位长度。
* 每个字节后必须跟随一个Ackknowledage位。
* 数据传输高位（MSB）在前
* 若从设备（Slave）未完成数据接收或需要进行其余操作，可将SCL拉低，让主设备（Master）进入等待状态。



### Acknowledge（ACK）和Not Acknowledge（NACK）

Acknowledge（ACK）发生在每个字节后。主设备（Master）产生所有的时钟周期，包括Acknowledge（ACK）第9个时钟。

* 当第9个时钟脉冲，SDA保持为LOW，产生Acknonwledge（ACK）信号。
* 当第9个时钟脉冲，SDA保持为HIGH，产生Not Acknowledge（NACK）信号。

receiver产生Acknowledge（ACK）来通知transmitter：字节接收完成，可进行下一字节的传输。

产生Not Acknowledge（NACK）的原因有5种：

* 对应地址不存在从设备。
* Receiver 因实时任务或无准备与主设备Master进行通讯，导致无法接收或传输。
* 在传输中，receiver接收到无法解析的指令或数据。
* 在传输中，receiver不能再接收更多的字节数据。
* **主设备作为receiver时，必须在传输的末字节后产生Not Acknowledge（NACK）**。

### Clock stretching

Clock stretching允许通过保持SCL总线为LOW暂停一个事务（transaction），直到SCL总线恢复为HIGH继续事务处理（transaction）。

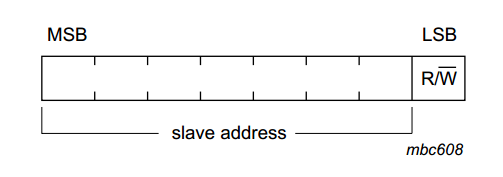
**NOTE**：

Clock stretching为可选项。

### 从机地址slave address和位

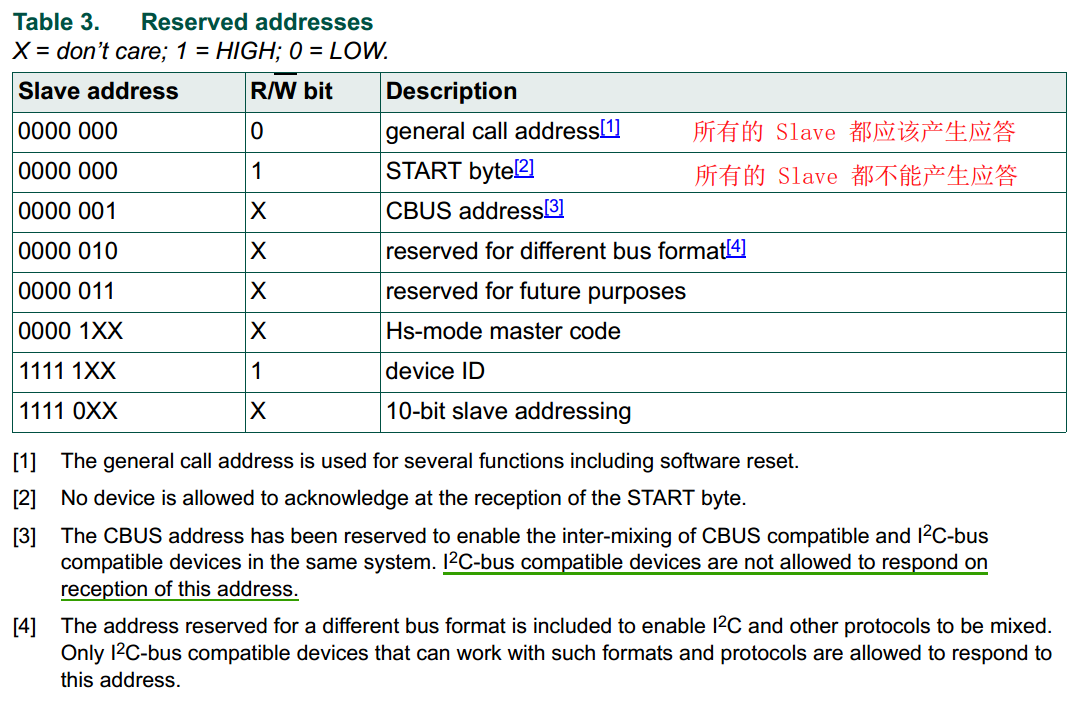
在START（S）信号后，主机将发生一个7bits的从机地址salve address，随后的第8bit为读写状态为位。

* 表示写（WRITE）操作。
* 表示读（READ）操作。



NOTE:

存在2组地址用于特殊用途，分别为000 XXX和1111 XXX。



### Software reset

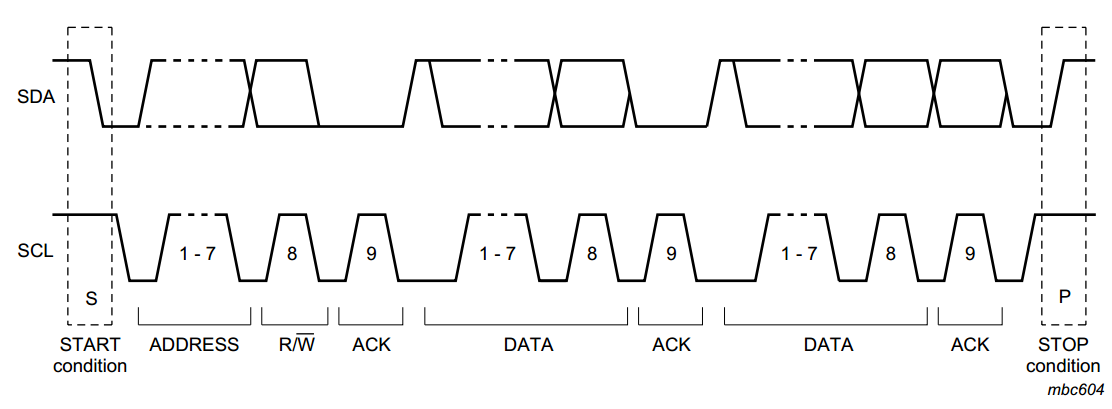
主机产生General Call（0000 0000）后，再发送0000 0110（06h）作为第二字节，将产生一次软件复位。

# 通讯过程

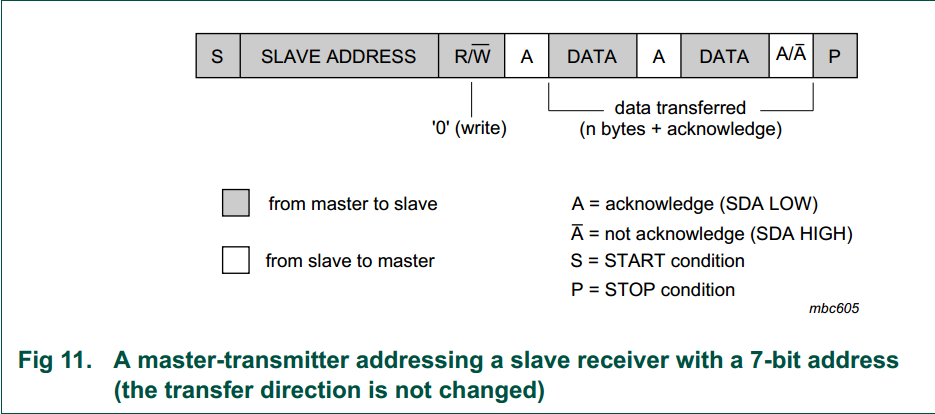
1. 主设备Master产生START信号
2. 主设备Master传输Slave address +
3. transmits发送数据，receiver产生ACK
4. 主设备Master产生STOP信号结束数据传输。

**NOTE**：

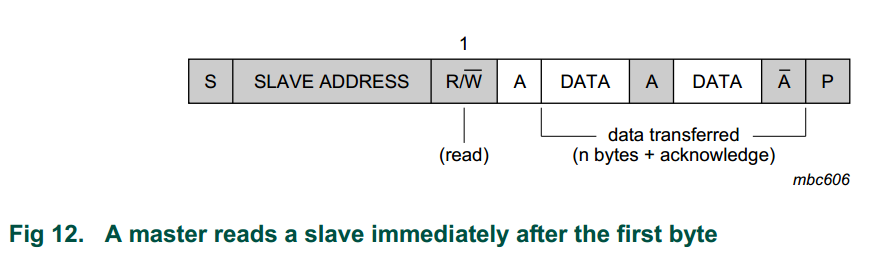
在数据传输结束后，主设备通常会产生STOP信号。若主机仍需要继续通讯，可以不先产生STOP信号，重新产生一个START信号和salve address。



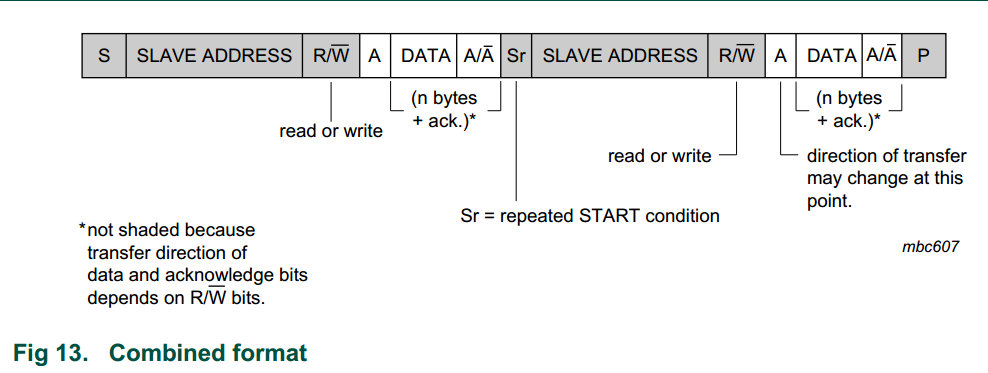
## A master-transmitter addressing a slave receiver with a 7-bit address



## A master reads a slave immediately after the first byte



## Combined format



# Bus speeds

|  |  |  |
| --- | --- | --- |
| **分类** | **传输速率** | **类型** |
| The Standard-mode（Sm） | up to 100 kbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Fast-mode（Fm） | up to 400 kbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Fast-mode Plus（Fm+） | up to 1 Mbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The High-speed mode（Hs-mode） | up to 3.4 Mbit/s | Serial, 8-bit oriented, bidirection data transfers |
| The Ultra Fast-mode（UFm） | up to 5 Mbit/s | Serial, 8-bit oriented, unidirection data transfers |

## Fast-mode

Fast-mode允许延长SCL总线的LOW周期来减速传输。The protocol,format,logic levels ,maximum capacitive load for SDA and SCL和The Standard-mode一样。

**NOTE**:

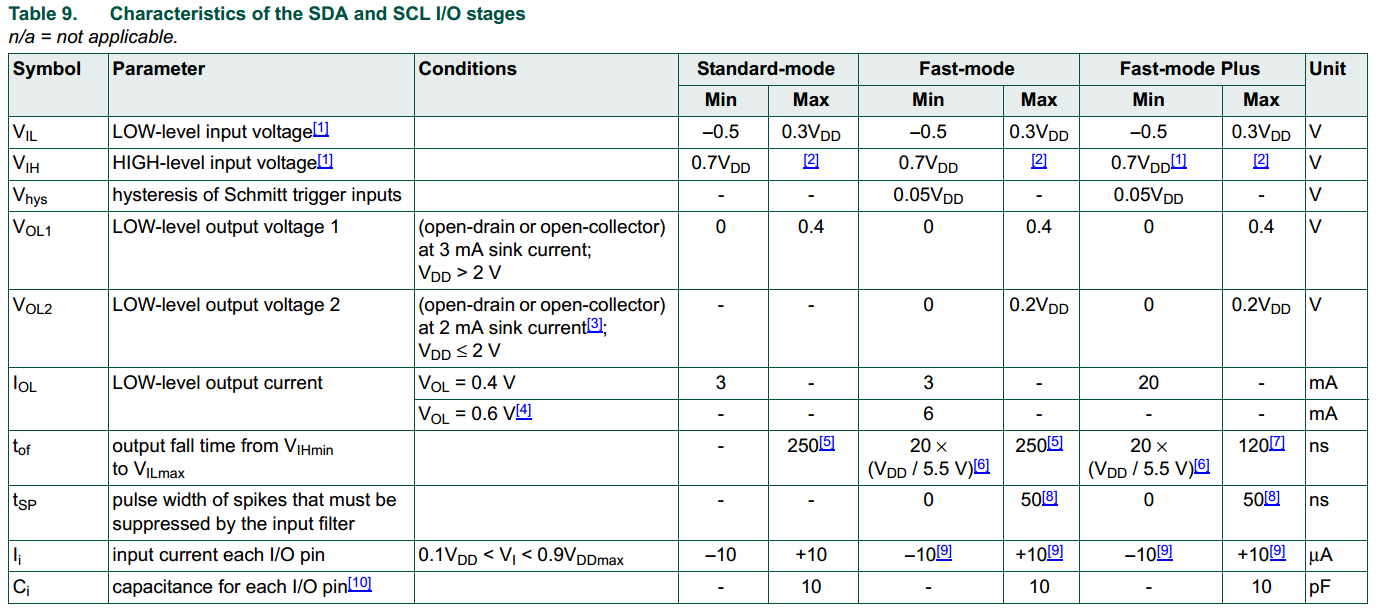
The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode IIC bus.

* For bus loads up to 200pF, the pull-up device for each bus line can be a resister.
* For bus loads between 200 pF and 400 pF, the pull-up decive can be a current source(3 mA max.) or a switched resistor circuit.

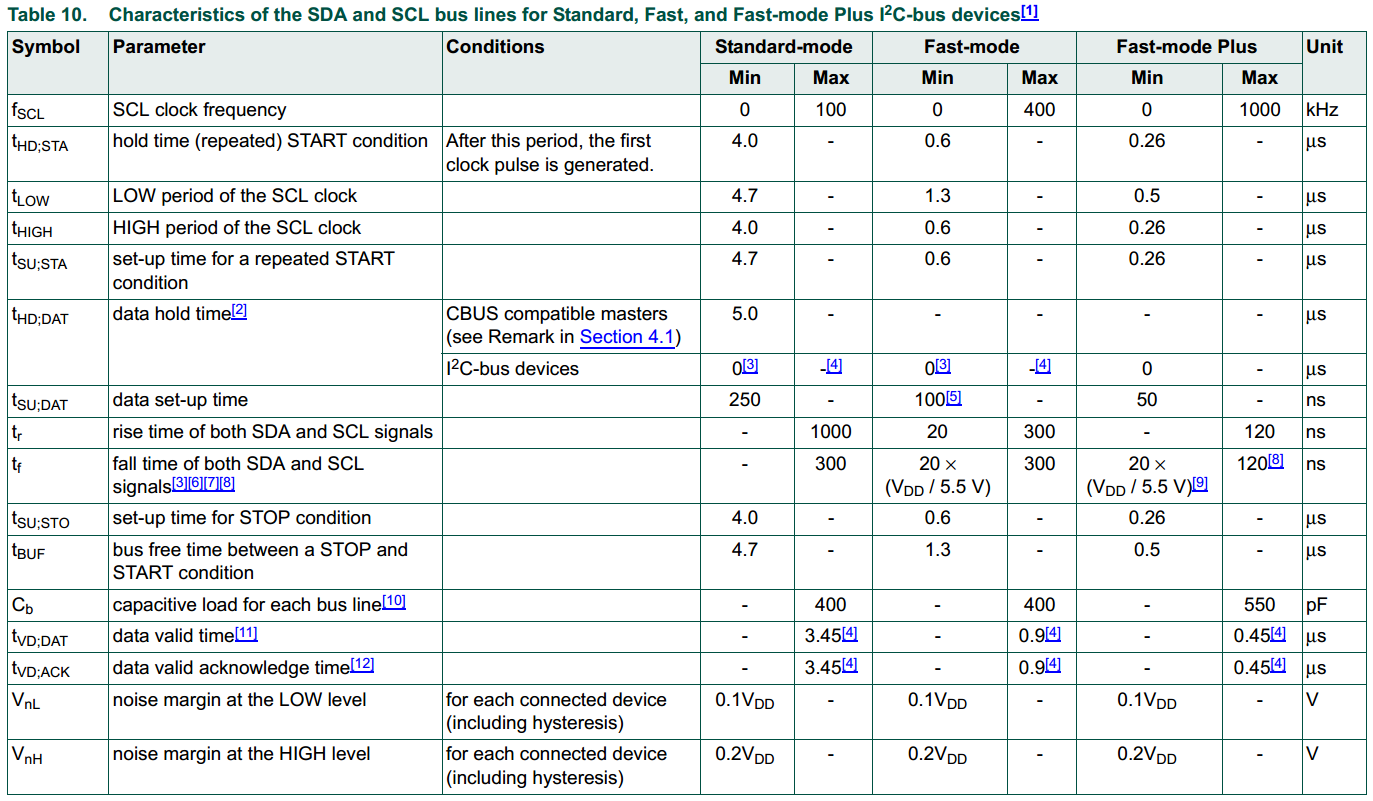
## Fast-mode Plus

The drivers in Fast-mode Plus parts are strong enough to satisfy the Fast-mode Plus  
timing specification with the same 400 pF load as Standard-mode parts. To be backward  
compatible with Standard-mode, they are also tolerant of the 1 μs rise time of  
Standard-mode parts. In applications where only Fast-mode Plus parts are present, the  
high drive strength and tolerance for slow rise and fall times allow the use of larger bus  
capacitance as long as set-up, minimum LOW time and minimum HIGH time for  
Fast-mode Plus are all satisfied and the fall time and rise time do not exceed the 300 ns tf  
and 1 μs tr specifications of Standard-mode. Bus speed can be traded against load  
capacitance to increase the maximum capacitance by about a factor of ten.

# Electrical specifications and timing for I/O stages and bus lines

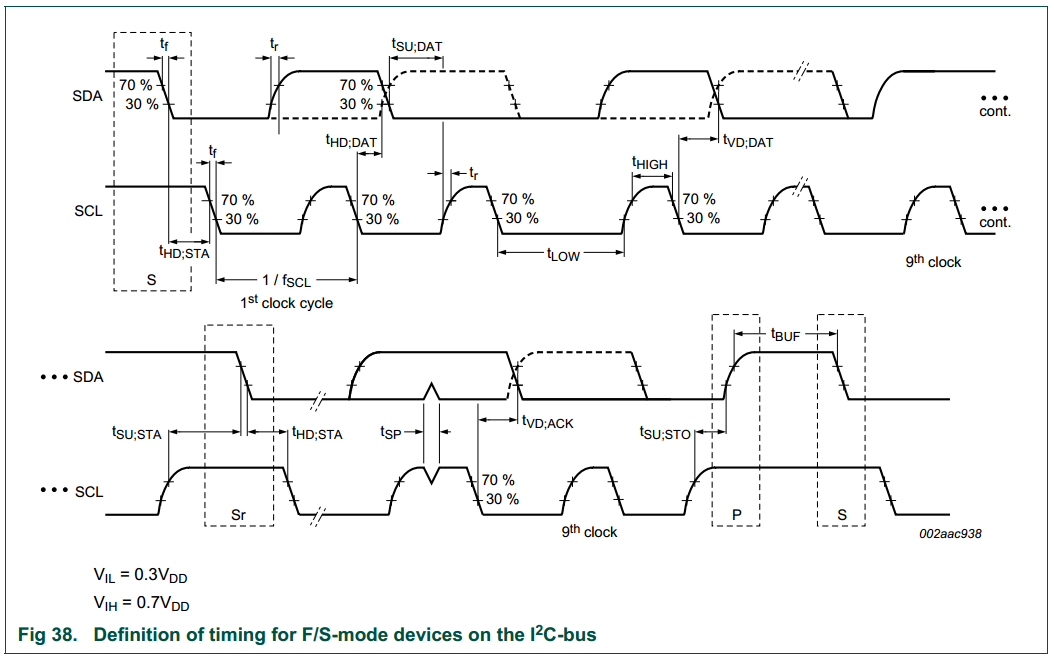


[1] Some legacy Standard-mode devices had fixed input levels of VIL = 1.5 V and VIH = 3.0 V. Refer to component data sheets.  
[2] Maximum VIH = VDD(max) + 0.5 V or 5.5 V, which ever is lower. See component data sheets.  
[3] The same resistor value to drive 3 mA at 3.0 V VDD provides the same RC time constant when using <2 V VDD with a smaller current draw.  
[4] In order to drive full bus load at 400 kHz, 6 mA IOL is required at 0.6 V VOL. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.  
[5] The maximum tf for the SDA and SCL bus lines quoted in Table 10 (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection  
resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Figure 45 without exceeding the maximum specified tf.  
[6] Necessary to be backwards compatible with Fast-mode.  
[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.  
[8] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.  
[9] If VDD is switched off, I/O pins of Fast-mode and Fast-mode Plus devices must not obstruct the SDA and SCL lines.  
[10] Special purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.



[1] All values referred to VIH(min) (0.3VDD) and VIL(max) (0.7VDD) levels (see Table 9).  
[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.  
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of  
SCL.  
[4] The maximum tHD;DAT could be 3.45 s and 0.9 s for Standard-mode and Fast-mode, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time. This maximum  
must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases  
the clock.

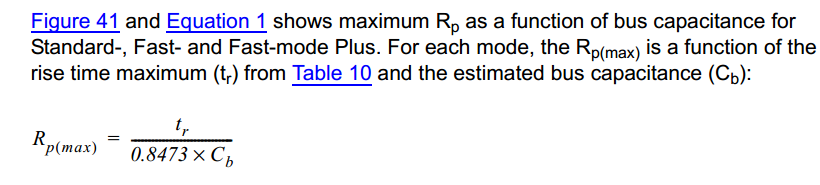
[5] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the  
device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  
tr(max) + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this  
set-up time.  
[6] If mixed with Hs-mode devices, faster fall times according to Table 10 are allowed.  
[7] The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage tf is specified at 250 ns. This allows series protection  
resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.  
[8] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.  
[9] Necessary to be backwards compatible to Fast-mode.  
[10] The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application. Section 7.2 discusses techniques  
for coping with higher bus capacitances.  
[11] tVD;DAT = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).  
[12] tVD;ACK = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

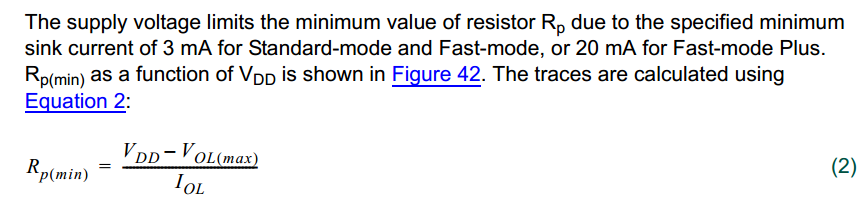


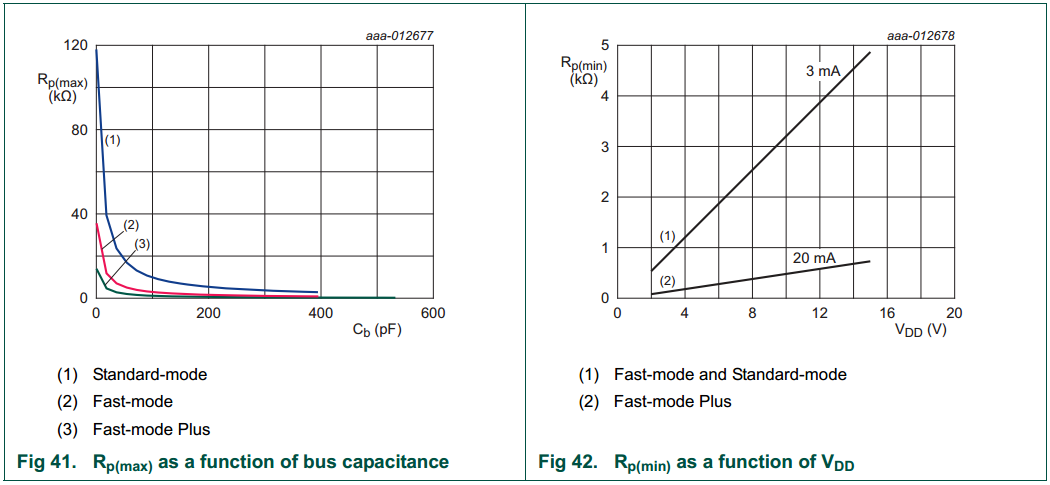
# Electrical connections of IIC-bus devices to the bus lines

## Pull-up resistor sizing

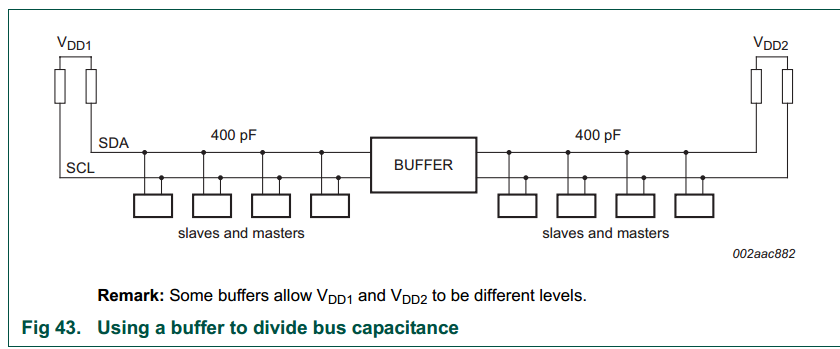
The bus capacitance is the total capacitance of wire, connections and pins. This  
capacitance limits the maximum value of Rp due to the specified rise time. Figure 41  
shows Rp(max) as a function of bus capacitance.  
Consider the VDD related input threshold of VIH = 0.7VDD and VIL = 0.3VDD for the  
purposes of RC time constant calculation. Then V(t) = VDD (1 et / RC), where t is the  
time since the charging started and RC is the time constant.  
V(t1) = 0.3 VDD = VDD (1 et1 / RC); then t1 = 0.3566749 RC  
V(t2) = 0.7 VDD = VDD (1 et2 / RC); then t2 = 1.2039729 RC  
T = t2 t1 = 0.8473 RC  
Figure 41 and Equation 1 shows maximum Rp as a function of bus capacitance for  
Standard-, Fast- and Fast-mode Plus. For each mode, the Rp(max) is a function of the  
rise time maximum (tr) from Table 10 and the estimated bus capacitance (Cb):





The designer now has the minimum and maximum value of Rp that is required to meet the  
timing specification. Portable designs with sensitivity to supply current consumption can  
use a value toward the higher end of the range in order to limit IDD  


## Bus buffers,multiplesers and switches



## Wiring pattern of the bus lines

